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Substitute for form 1449A/PTO		<b>Compleat if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Application Number	<del>TBD</del> 10/771,075
		Filing Date	HEREWITH 2/03/2004
		First Named Inventor	U
		Art Unit	<del>TBD</del> 2811
		Examiner Name	<del>TBD</del> G. MUNSON
Sheet 1 of 1	Attorney Docket Number	2003 P 54557 US	

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>3</sup>
		Country Code <sup>2</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

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Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
<i>R/K/K</i>	1	INUMIYA, S., et al., "Fabrication of HfSiON Gate Dielectrics by Plasma Oxidation and Nitridation, Optimized for 65nm node Low Power CMOS Applications," 2003 Symposium on VLSI Technology Digest of Technical Papers, pp. 18-19, Document No. 4-89114-035-6/03.	
<i>R/K/K</i>	2	WOLF, S., "Silicon Processing for the VLSI Era: Diffusion in Silicon" pp. 336-339.	

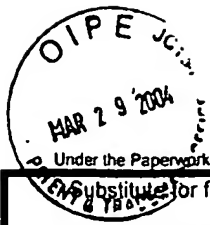
Examiner Signature	G. MUNSON	Date Considered	25 FEBRUARY 2005
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	10/771,075
				Filing Date	February 3, 2004
				First Named Inventor	Li
				Art Unit	18D 2811
				Examiner Name	18D G. MUNSON
				Attorney Docket Number	2003 P 54557 US
Sheet	1	of	1		

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	1	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2003 Edition, pp. 23-25, <a href="http://member.itrs.net/">http://member.itrs.net/</a> .	

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